The embodiments of the invention in which an exclusive property or privilege is claimed are defined as follows:

1. An active pixel sensor circuit, comprising:

a sensor for producing a sensor potential;

a pull-down circuit for implementing a pull down function during which the sensor potential is pulled down below a selected critical level;

a reset voltage line coupled to the pull-down circuit; and

a reset transistor coupled between the reset voltage line and the sensor, wherein during the pull down function the reset transistor is conducting and the pull-down circuit operates to pull down the sensor potential below the selected critical level, the pull down function being performed prior to the completion of a reset function when the sensor potential is reset to a selected level.

2. The active pixel sensor circuit of Claim 1, wherein the pull-down circuit places a first low voltage level on the reset voltage line, and then places a second high voltage level on the reset voltage line after the sensor potential has been pulled below the selected critical level.

3. The active pixel sensor circuit of Claim 2, wherein the pull-down circuit places the first low voltage level on the reset line while the reset transistor is conducting, and the pull down function is made to be shorter than the total time that the reset transistor is conducting.

4. The active pixel sensor circuit of Claim 2, wherein the first low voltage level is approximately at the ground level.

5. The active pixel sensor circuit of Claim 2, wherein the first low voltage level is above the ground level but below the selected critical level.

6. The active pixel sensor circuit of Claim 1, wherein the pull-down circuit comprises a PMOS transistor.

7. The active pixel sensor circuit of Claim 6, wherein the pull-down circuit further comprises an NMOS transistor, the NMOS and PMOS transistors of the pull-down circuit being coupled together as a CMOS inverter.

8. The active pixel sensor circuit of Claim 1, wherein the pull-down circuit comprises a bit line, wherein the bit line is coupled to the sensor during the pull down function to pull the sensor potential below the selected critical level.

9. The active pixel sensor circuit of Claim 8, further comprising a loading transistor coupled to the bit line, and a biasing circuit coupled to the loading transistor for generating the bias on the loading transistor, wherein the voltage level on the bit line is pulled down during the pull down function by the biasing circuit increasing the bias on the loading transistor.

10. The active pixel sensor circuit of Claim 8, further comprising a loading transistor coupled to the bit line, and an NMOS pull-up transistor coupled to the loading transistor, wherein the voltage level on the bit line is pulled down during the pull down function by the NMOS pull-up transistor increasing the bias on the loading transistor.

11. The active pixel sensor circuit of Claim 8, further comprising a loading transistor coupled to the bit line, and a PMOS pull-up transistor coupled to the loading transistor, wherein the voltage level on the bit line is pulled down during the pull down function by the PMOS pull-up transistor increasing the bias on the loading transistor.

12. The active pixel sensor circuit of Claim 8, wherein the voltage level on the bit line is pulled down during the pull down function by natural discharge.

13. The active pixel sensor circuit of Claim 1, wherein the sensor comprises a photodiode, photogate or pinned diode.

14. The active pixel sensor circuit of Claim 1, wherein the selected critical level is determined according to the potential at which the reset transistor will be on when the reset function starts.

15. The active pixel sensor circuit of Claim 1, wherein the timing of the pull down function is such that the sensor is stabilized at a level below the selected critical level before the reset function starts.

16. A method for implementing a soft reset in an active pixel sensor, the active pixel sensor including a sensor which produces a sensor potential and a reset transistor coupled to the sensor, the method comprising:

(a) determining a selected critical level according to the critical potential at which the reset transistor will be on when the soft reset function begins;

(b) pulling down the sensor potential below the selected critical level before the soft reset function is performed; and

(c) implementing the soft reset function to reset the sensor potential to a selected reset level.

17. The method of Claim 16, wherein during step (b) the sensor potential is stabilized below the critical level before the soft reset begins at step (c).

18. The method of Claim 16, wherein the sensor potential is pulled down by a pull-down circuit.

19. The method of Claim 18, wherein the pull-down circuit comprises an NMOS transistor and a PMOS transistor coupled together in the form of a CMOS inverter.

20. The method of Claim 16, wherein the sensor is coupled through a plurality of transistors to a bit line, and the bit line is used to pull down the sensor potential.

21. The method of Claim 20, wherein a loading transistor is coupled to the bit line, and the voltage potential on the bit line is pulled down by increasing bias on the loading transistor.

22. The method of Claim 21, wherein the gate of the loading transistor is coupled to a biasing circuit, and the biasing circuit is used to increase the bias on the loading transistor.

23. The method of Claim 21, wherein a pull-up transistor is coupled to the gate of the loading transistor, and the pull-up transistor is used to increase the bias on the loading transistor.

24. An active pixel sensor circuit in which a soft reset function is performed, the active pixel sensor circuit comprising:

a sensor which outputs a sensor potential;

a reset transistor coupled to the sensor;

a bit line coupled through a plurality of transistors to the sensor, wherein the sensor potential is pulled below a selected critical level prior to the time when a soft reset function is performed to reset the sensor potential.

25. The active pixel sensor circuit of Claim 24, further comprising a reset voltage line coupled to the reset transistor, a signal path existing between the reset voltage line and the sensor when the reset transistor is biased in a conducting state.

26. The active pixel sensor circuit of Claim 25, further comprising a CMOS inverter circuit coupled through the reset voltage line to the reset transistor for pulling down the sensor potential below the selected critical level.

27. The active pixel sensor circuit of Claim 24, wherein the bit line is used to pull the sensor potential below the selected critical level.

28. The active pixel sensor circuit of Claim 27, wherein the bit line is coupled to a loading transistor, the voltage potential on the bit line being pulled down by increasing the bias on the loading transistor.

29. The active pixel sensor circuit of Claim 28, further comprising a biasing circuit coupled to the loading transistor, the biasing circuit being used to increase the bias on the loading transistor so as to pull down the voltage level on the bit line.

30. The active pixel sensor circuit of Claim 28, further comprising a pull-up transistor coupled to the gate of the loading transistor, the pull-up transistor increasing the bias on the loading transistor so as to pull down the voltage potential on the bit line.

31. The active pixel sensor circuit of Claim 24, wherein the selected critical level is determined according to the potential at which the reset transistor will be on when the soft reset function begins.